

Serial No. 10/673,459

HIT 844-05

IN THE CLAIMS

Claims 1-34 (Canceled)

35. (Previously Presented) A method of manufacturing a semiconductor device, comprising the steps of:

electrically connecting together each of a plurality of semiconductor chips with a respective base member having a circuit wiring; and

resin-sealing said plurality of said semiconductor chips at a time,

wherein said step of resin-sealing is carried out after positioning a frame that supports said base member between an upper half of a mold and a lower half thereof.

36. (Previously Presented) The manufacturing method according to claim 35, further comprising the step of forming solder bumps on said resin-sealed semiconductor chip.

37. (Previously Presented) The manufacturing method according to claim 36, further comprising the step of separating individual ones of said plurality of semiconductor chips.

38. (Previously Presented) The manufacturing method according to claim 37, wherein said step of resin-sealing is

Serial No. 10/673,459

HIT 844-05

conducted in such a manner that a surface on which said solder bumps are formed is resin-free.

39. (Previously Presented) The manufacturing method according to claim 35, wherein said base member includes an insulating base member and wiring patterns formed on first and second opposing surfaces of said insulating base member, said wiring patterns on said first and second surfaces of said insulating base member are electrically connected to each other, said semiconductor chip is mounted on said first surface of said base member, and solder bumps are formed on the second surface of said base member.

40. (Previously Presented) The manufacturing method according to claim 35, wherein in said resin-sealing step, said plurality of semiconductor chips are transfer molded.

41. (Previously Presented) The manufacturing method according to claim 35, wherein in said step of electrically connecting together said semiconductor chips and said base members, each of said semiconductor chip and base member are connected by a wire bonding, no electrical connection is made between said frame and said semiconductor chips, and no electrical connection is made between said frame and said base members.

Serial No. 10/673,459

HIT 844-05

42. (Previously Presented) The manufacturing method according to claim 35, wherein said base member is a multi-layered circuit board.

43. (Previously Presented) The manufacturing method according to claim 35, wherein said base member is a circuit film.

**This Page is Inserted by IFW Indexing and Scanning
Operations and is not part of the Official Record**

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images include but are not limited to the items checked:

- ☐ BLACK BORDERS
- ☐ IMAGE CUT OFF AT TOP, BOTTOM OR SIDES
- ☐ FADED TEXT OR DRAWING
- ☐ BLURRED OR ILLEGIBLE TEXT OR DRAWING
- ☐ SKEWED/SLANTED IMAGES
- ☐ COLOR OR BLACK AND WHITE PHOTOGRAPHS
- ☐ GRAY SCALE DOCUMENTS
- ☒ LINES OR MARKS ON ORIGINAL DOCUMENT
- ☐ REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY
- ☐ OTHER: _____

IMAGES ARE BEST AVAILABLE COPY.

As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.